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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,113	12/13/2001	Andrew Marshall	TI-31157	2385

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,113	MARSHALL ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Response to Applicant's Arguments

Applicant's arguments filed 09/08/2003 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

1. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Nishihara et al. (U.S. Pub. 2002/0137320).

In re claims 1 and 17, **Nishihara** discloses a method of forming a semiconductor circuit (memory configuration), comprising the steps of (see page 4, paragraph [0071] to page 5, paragraph [0079] and **FIGS. 1-7**):

forming a first transistor, comprising the steps of:

forming a first source/drain region (**14** on the left side) as a first doped region in a fixed relationship to a semiconductor substrate **1**;

forming a second source/drain region (**14** on the right side) as a second doped region **14** in a fixed relationship to the semiconductor substrate **1**, wherein the second doped region and the first doped region are of a same conductivity type;

forming a first gate **8n** in a fixed relationship to the first source/drain region and the second drain region; and

forming a second transistor, comprising the steps of:

forming a third source/drain region (**13** on the left side) as a third doped region in a fixed relationship to the semiconductor substrate **1**;

forming a fourth source/drain region (**13** on the right side) as a fourth doped region in a fixed relationship to the semiconductor substrate **1**, wherein the fourth doped region and the third doped region are of the same conductivity type as the first and second doped regions;

forming a second gate **8p** in a fixed relationship to the third source/drain region and the fourth drain region; and

wherein the steps of forming the first gate and the second gate comprise forming the first gate to comprise a first dopant concentration and forming the second gate to comprise a second dopant concentration different from the first dopant concentration (page 5, paragraph [0079] and **FIG. 7**).

In re claims 2 and 17, **Nishihara** discloses wherein the steps of forming the first **8n** and the second gate **8p** further comprise: forming a semiconductor layer **8** in a fixed relationship to the semiconductor substrate **1**; in an implant step, selectively implanting dopants into a portion of the semiconductor layer in an area corresponding to the first

transistor while not implanting dopants into a portion of the semiconductor layer in an area corresponding to the second transistor and selectively implanting dopants into a portion of the semiconductor layer in an area corresponding to the second transistor such that the area has a first dopant concentration while not implanting dopants into a portion of the semiconductor layer in an area corresponding to the first transistor in each cell (page 5, paragraph [0079] and **FIG. 7**).

In re claims 3-5 and 13, **Nishihara** discloses wherein the steps of forming the first gate 8n and the second gate **8p** further comprises patterning and etching the semiconductor layer **8** to form the first gate form the area corresponding to the first transistor and the second gate from the area corresponding to the second transistor wherein the semiconductor layer comprises polysilicon and wherein the step of forming a semiconductor layer comprises forming a polysilicon layer with an in-situ doping (page 5, paragraph [0076] and **FIG. 6**).

In re claims 6, 12 and 16, **Nishihara** discloses wherein the in-situ doping comprises p-type in-situ doping; and wherein the first, second, third, and fourth doped regions comprises n-type doped regions (page 5, paragraph [0079] and **FIG. 7**).

In re claims 7 and 18, Nishihara discloses wherein the first transistor has a first threshold voltage in response to the first dopant concentration; and wherein the second transistor has a second threshold voltage in response to the second dopant concentration and such that the second threshold voltage is greater or less than the first threshold voltage (pages 4-5, paragraph [0074]).

In re claims 8-9, and 19, **Nishihara** discloses wherein the second transistor comprises a state transistor in a memory cell wherein the state transistor comprises a first state transistor; and further comprising the step of forming a second state transistor in the memory cell, comprising the step of forming a third gate corresponding to the second state transistor and comprising the second dopant concentration (pages 4-5, paragraph [0074] and **FIGS. 1-7**).

In re claims 10 and 20, **Nishihara** discloses forming a first access transistor in the memory cell, the first access transistor coupled and operable to read a state from, and write a state to, a source/drain of the first state transistor; and forming a second access transistor in the memory cell, the second access transistor coupled and operable to read a state from, and write a state to, a source/drain of the second state transistor (pages 4-5, paragraph [0074] and **FIGS. 1-7**).

In re claim 11, **Nishihara** discloses wherein the first and second access transistors comprise source/drain regions of a conductivity type that is complementary of source/drain regions of the first and second state transistors (pages 4-5, paragraph [0074] and FIGS. 1-7).

In re claims 14-15, **Nishihara** discloses wherein the first transistor comprises a transistor in a sense amplifier.

2. Claims 21-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Nishihara et al. (U.S. Pub. 2002/0137320).

Nishihara discloses a semiconductor circuit (memory configuration), comprising (see page 4, paragraph [0071] to page 5, paragraph [0079] and **FIGS. 1-7**):

a plurality of memory cells, wherein each of the memory cells comprises

a first transistor, comprising:

a first source/drain region (**14** on the left side) comprising a first doped region in a fixed relationship to a semiconductor substrate **1**;

a second source/drain region comprising a second doped region (**14** on the right side) in a fixed relationship to the semiconductor substrate **1**, wherein the second doped region and the first doped region are of a same conductivity type;

a first gate **8n** in a fixed relationship to the first source/drain region and the second drain region; and

the memory configuration further comprising a second transistor outside of the plurality of memory cells, comprising:

a third source/drain region (**13** on the left side) comprising a third doped region in a fixed relationship to the semiconductor substrate **1**;

a fourth source/drain region (**13** on the right side) comprising a fourth doped region in a fixed relationship to the semiconductor substrate **1**, wherein the fourth doped region and the third doped region are of the same conductivity type as the first and second doped regions;

a second gate **8p** in a fixed relationship to the third source/drain region and the fourth drain region; and

wherein the first gate for each cell in the plurality of memory cells comprises a first dopant concentration and the second gate comprises a second dopant concentration different from the first dopant concentration wherein the first gate comprises a first

dopant concentration that is less than a dopant concentration in the second gate (page 5, paragraph [0079] and **FIG. 7**).

Response to Amendment

Response to Applicant's Arguments

Applicant's arguments filed 09/08/2003 have been fully considered but they are not persuasive.

Applicants contend that Nishihara fails to meet the limitations of the claimed invention because Applicants state that the different doping requirement of claim 1 is not found in the cited art.

In response to Applicant's contention that the different gate doping requirement of claim 1 is not found in the cited art, examiner respectfully disagree, it is well known that semiconductor substrates and wells formed in semiconductor substrate require distinct doping concentrations, which are clearly shown by Nishihara. Because Applicant's do not further limit claim 1 beyond the terms "first dopant concentration" and "second dopant concentration" Nishihara teaches Applicant's claimed invention. Applicant's claims are not enforceable over the prior art.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
November 4, 2003

W. David Coleman
Primary Examiner